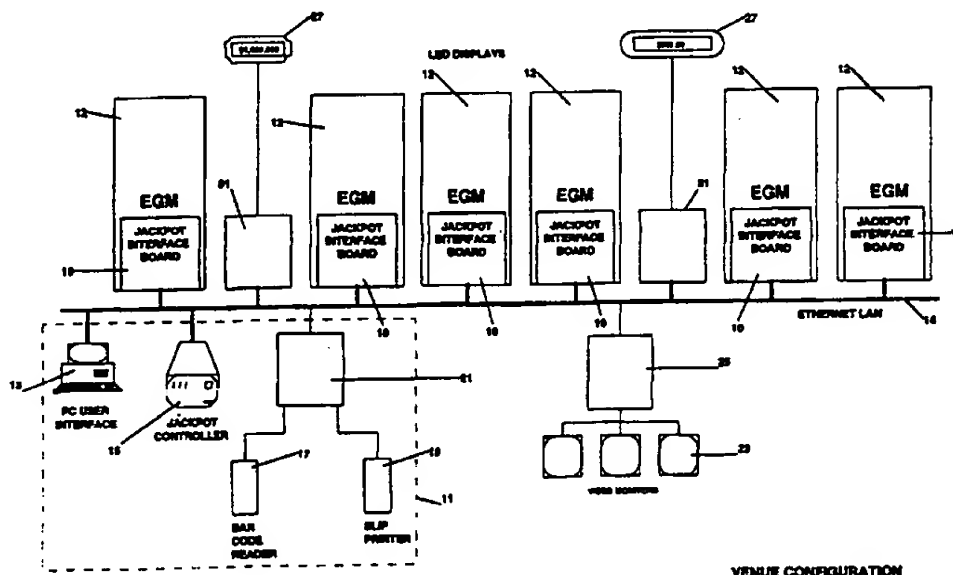




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 3/14, H07N 5/262, A63F 9/22, G06F 19/00, 161/00		A1	(11) International Publication Number: WO 97/12315
		(43) International Publication Date: 3 April 1997 (03.04.97)	
(21) International Application Number: PCT/AU96/00609		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 26 September 1996 (26.09.96)		Published With international search report.	
(30) Priority Data: PN 5642 26 September 1995 (26.09.95) AU			
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(54) Title: JACKPOT DISPLAY SYSTEM FOR AN ELECTRONIC GAMING MACHINE



(57) Abstract

Jackpot interface (10) connects to electronic gaming machines (12) (i.e. poker, slot, video machines) which include hard meters (6) and video displays (23, 27). The gaming machines (12) are capable of playing independent games and participating in a multiple gaming machine jackpot game. The gaming machines (12) are connected to a LAN (14). Included is a video display generator which on a jackpot award replaces or superimposes on a first video signal a second video signal that it generates. A jackpot controller (15) increments on the basis of the hard meter (6) signals and/or awards a jackpot sum from a jackpot pool to a selected gaming machine (12). The interface (10) stops independent play of the gaming machine (12) upon a jackpot award. The jackpot interface (10) is a separate circuit board capable of being fitted to a standard gaming machine (12).

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JACKPOT DISPLAY SYSTEM FOR AN ELECTRONIC GAMING MACHINE

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This invention relates to an electronic gaming machine (EGM) which is capable of playing normal games such as poker, blackjack or other gambling games and which is also capable of participating in a jackpot involving a number of participating EGMs.

10 Most EGMs have a video display and EGM logic which generates video signals for displaying information relevant to the playing of the normal game on the video displays. The EGMs also usually include hard meters which indicate such things as the credit played (which is the amount of cash which has been wagered), cash out (which is the amount of cash paid out by the EGM), cash in (which is the amount of cash inserted into the machine) and credit
15 won (which is the amount of money which has been won on that machine). The EGM logic is arranged to produce hard meter input signals for driving the hard meters.

In accordance with the invention, the EGM includes a jackpot interface board which is responsive to the hard meter output signal in order to allow the EGM to participate in a
20 jackpot game involving a number of EGMs linked together, the interface board also including means for generating video signals relevant to the jackpot, the arrangement being such that the jackpot signals can be superimposed on or replace the normal display.

More particularly, the invention provides a jackpot interface for connection to an
25 electronic gaming machine (EGM) which includes a video display, a hard meter, and EGM logic for generating first video signals for said video display and hard meter input signals for said hard meter, said EGM being adapted to play an independent game and participate in a multiple EGM jackpot game, wherein the jackpot interface comprises:

a hard meter monitor which monitors said hard meter input signals for communication
30 to a controller for determination of a jackpot award;

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video generating means for generating second video signals relating to said jackpot award; and

combining means for causing the second video signals to be superimposed on or replace the first video signals to thereby display on said video display messages relating to
5 said jackpot award.

Preferably, the combining means comprises a video multiplexing device which receives said first and second video signals and its output is coupled to said video display.

10 Preferably further, the EGM includes at least one EGM disable circuit (such as a door open circuit) for generating disable signals wherein the EGM logic is responsive to said disable signals to stop playing of normal games when a door is opened. Preferably the jackpot interface board includes logic circuitry for generating, when a jackpot has been won, a signal which is transmitted to the EGM logic and which is interpreted by the EGM logic as a disable
15 signal, thereby stopping normal game play on the EGM.

The invention also provides a jackpot interface board for use in an EGM having a video display, hard meters and EGM logic for generating first video signals for said video display and hard meter input signals to said hard meters, said jackpot interface board including
20 monitoring means for monitoring hard meter input signals generated by the EGM logic and transferring said hard meter input signals for addition to a jackpot pool for determining when a jackpot pool is won, video generating means for generating jackpot video signals and video combining means for causing said jackpot video signals to be superimposed upon the video display when a jackpot has been won.

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The invention will now be further described with reference to the accompanying drawings, in which:

Figure 1 is a schematic block diagram of an EGM network having a number of EGMs of the invention incorporated therein;

30 Figure 2 schematically illustrates an EGM;

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Figure 3 schematically shows some of the components of an EGM;

Figure 4 shows an interface board of the invention connected to an EGM;

Figure 5 is a block diagram of an interface board;

Figures 6 to 10 are a detailed circuit diagram of the video interface board shown in

5 Figure 5;

Figures 11 to 14 are block diagrams of the logic circuitry shown in Figure 7;

Figure 15 is an example of the coupling of the interface board to one form of EGM;

Figure 16 is a flow chart showing boot loading of the interface boards; and

Figures 17 and 18 are flow charts showing main operating loops for the software in the
10 interface board.

Figure 1 diagrammatically illustrates a plurality of EGMs 12 coupled together by means of a venue jackpot network 14. This network is preferably additional to any existing network linking the EGMs together at a venue. The venue jackpot network 14 may comprise
15 an ethernet LAN of known type and therefore need not be described in detail. Each of the EGMs 12 is connected to the venue jackpot network 14 via a jackpot interface board 10. The system includes jackpot control station 11 having control devices which are coupled to the venue jackpot network 14 so as to provide various forms of control to the EGMs 12 via the jackpot interface boards (JIBs) 10. The jackpot control station 11 includes a PC user interface
20 13 which operates as an input/output terminal by which an operator can control various aspects of the system. A jackpot controller 15 is coupled to the venue jackpot network 14 and essentially provides input and output signals to the venue jackpot network 14 relating to a particular jackpot which may be implemented in the system. The jackpot controller 15 may be implemented in a number of ways, such as a computer having the necessary data handling
25 capabilities. The preferred implementation is to use a Motorola MVME 162 LX embedded controller. These devices include memory and a processor which can provide the necessary input and output signals for carrying out a jackpot on the EGMs 12. The embedded controller device is fitted with an ethernet controller which enables ready coupling to the venue jackpot network 14. An example of the jackpot controller 15 is described in greater detail in a
30 copending Australian application filed contemporaneously herewith in respect of an invention

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entitled MULTIVENUE JACKPOT SYSTEM and the content of that application is incorporated herein by reference.

The jackpot control station 11 may include other peripheral devices such as a bar code reader 17 and card printer 19 coupled to the venue jackpot network 14 by means of a peripheral interface board 21. The system may include a number of video monitors 23 which are coupled to the venue jackpot network 14 by means of a video display interface 25. Finally, the system may include a number of large LED displays 27 which are coupled to the venue jackpot network 14 by means of LED display interfaces 31. The monitors 23 and LED displays 27 display prize money or other information relative to the jackpot.

Each of the EGM devices has its own internal video display (Figure 2) and input and output devices by which the user can operate the EGM machine in the usual way. During the course of playing of the EGM machines, a jackpot can be activated according to parameters determined by the jackpot controller 15.

When an event occurs corresponding to the winning of a jackpot, jackpot signals will be transmitted to the jackpot controller 15 by the EGM triggering the win. The jackpot controller 15 will then generate signals which are applied to the venue jackpot network 14. The signals will be received by the jackpot interface boards 10 of the various EGMs and on receipt of these signals the normal video display of the EGM has superimposed thereon information relating to the winning of the jackpot. The superimposed information can be restricted to the particular EGM which triggered the jackpot win or alternatively could be displayed on all or a selected number of the EGMs in the system. Whilst it is preferred that while the jackpot video information is being displayed the normal EGM display is blanked out, an arrangement in which the jackpot video information is superimposed on the normal EGM display could also be implemented.

Figure 2 diagrammatically illustrates a typical EGM 12. It has a cabinet 1 in which is mounted an EGM display 2. The cabinet has control buttons 3 and optionally an operating

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lever 4 by which the user can make appropriate selections for playing a game. The cabinet includes a money tray 5 to which coins can be dispensed when a win occurs. Located within the cabinet 2 are four hard meters 6 which typically register parameters such as the amount of cash in, cash won, cash out and credit played. The EGM includes EGM logic circuitry 7 which controls the normal playing operation of the EGM and handles various inputs and outputs for playing the machine, as is well understood in the art. For security reasons, the hard meters 6 can only be accessed when an authorised operator opens a door 8 and this will trigger a door seal switch 9 located in the cabinet. Similarly, the EGM logic 7 is located within a sealed compartment which is provided with a logic seal switch 41. The EGM 12 may also include an audit key 43 which enables an operator to carry out auditing and maintenance on the EGM. The states of the switches 9 and 41 and the key 43 are monitored by the EGM logic 7 and usually operate to disable the normal running of the EGM when the doors have been open or the audit key turned. Usually this is accompanied by an appropriate message on the EGM display 2.

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Figure 3 is a block diagram of the basic electric circuits of the EGM. Figure 4 shows the way in which the jackpot interface board 10 is added. It will be seen that the interface board 10 is interposed between the EGM logic 7 and the EGM display 2. The interface board 10 is also interposed between the EGM logic 7 and the hard meters 6. In addition, the interface board 10 is effectively connected in series with the logic seal switch 41 and audit key 43. Thus the EGM logic 7 as well as the interface board 10 are responsive to changes in the states of the switch 41 and key 43. The door seal switch 9 is inputted to the EGM logic 7 via the interface board 10 which includes relay contacts 45 effectively connected in series with the door seal switch 9. This provides a very simple and effective coupling between the interface board 10 and the EGM logic 7. As will be described in more detail hereinafter, when a jackpot has been won on an EGM, the board 10 needs to provide appropriate input signals to the EGM to prevent further game play. In the preferred embodiment of the invention, this is done by opening the relay contacts 45 which provides a signal to the EGM logic which is effectively the same as that when the door seal switch 9 is opened. The EGM logic 7 is programmed to stop play when this occurs, in the usual way.

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Figure 5 diagrammatically illustrates a video superposition interface board 10 constructed in accordance with the invention. The interface board 10 carries out a variety of functions. Its main function, however, is to enable the EGM 12 to which it is connected to participate in a jackpot game involving a number of EGMs 12 which are linked together, as shown in Figure 1. In order to permit this, the board 10 permits the jackpot controller 15 to monitor inputs to the hard meters 6 of the EGM. It also permits the jackpot controller to check the status of the logic seal switch 41, the audit key 43 and the door seal 9. It also superimposes messages on the EGM display 2 relevant to the jackpot.

10 The board 10 comprises a microprocessor 16, a serial communications port 18 (or a pair of serial ports), a memory 20 and a network interface 22. The board 10 includes a system bus 78 coupled between the microprocessor 16 and the network interface 22. The network interface 22 may comprise known forms of interface device such as "ethernet" cards or the like such as an AT/LANTIC DP83905 device, for example. The network interface 22 is
15 coupled to the venue jackpot network 14 by means of a connector 72. Data flows between the EGM and the venue jackpot network 14 through the interface device and is formatted by the microprocessor 16 by reference to stored information in the memory 20. The memory 20 may for example comprise a flash ROM and battery backed RAM so as to be able to retain data without need for continued electric supply thereto. The memory 20 contains software for
20 implementation of processing steps by the microprocessor relating to jackpot implementation and video displays.

The board 10 also includes a serial communications bus 28 which can allow communications through the serial communications port 18 via connectors 108 and 110.

25

The interface board 10 also includes a video mixing device 42. This is able to receive video in data from the EGM logic 7 and provide video out data for the EGM display 2 via video in and video out connectors 140 and 144 respectively. The device 42 is coupled to the microprocessor 16 which provides a control mechanism for controlling video mixing of video
30 signals applied to the EGM display 2. The device 42 is preferably arranged to superimpose

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jackpot information on the normal display of the EGM. Alternatively, it can be arranged to blank out the normal display messages provided by the EGM logic 7 and display only jackpot information which is derived through signals from the interface board 10. The video mixing device 42 is coupled to the microprocessor 16 so that the microprocessor has control over the
5 function of the mixing device 42.

The jackpot parameters, such as for example the upper limit, lower limit, percentage contribution, restart value, etc., are stored in the jackpot controller 15. In some systems this information may be transmitted to the jackpot controller from a remote location or
10 alternatively it could be inputted at the jackpot control station 11. When the jackpot interface board 10 comes on line corresponding to an EGM being played, the jackpot controller 15 transmits the jackpot configuration to the jackpot interface board 10. Thus, each jackpot interface board 10 will receive the configuration, store it in the memory 20, the board then sending an acknowledgment to the jackpot controller 15. If a jackpot interface board 10 is
15 already on line, a new configuration can be transmitted to it by the jackpot controller 15. Once a jackpot interface board 10 receives the configuration, it preferably overlays an identifying number on the EGM display 2.

Once the configuration of a jackpot has been completed, a start command can be issued
20 to the jackpot controller 15 from the PC user interface 13 or from a remote centre, it checks for all the vital information that is required to run the jackpot. The jackpot controller 15 then generates a hidden prize between the low limit and high limit and sends the hidden prize value to the PC user interface 13 or to the remote centre and thereafter the jackpot controller activates the jackpot interface boards 10 which are participating in the jackpot. This is
25 achieved by broadcasting a jackpot open command together with an appropriate message to be displayed on the EGM displays 2 as well as to other displays such as the video monitors 23 and the LED displays 27. This is most efficiently achieved by setting up the messages on the jackpot interface boards 10 during the configuration phase, each message having a unique message ID so that the jackpot controller 15 need only broadcast the message ID in order for
30 the appropriate message to be displayed. The jackpot interface boards 10 will then overlay

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the message on the EGM displays 2. The jackpot controller creates a jackpot pool and a hidden prize value and calculates the amount that is required to be contributed in order to hit the hidden value.

5 For every \$1 that is played on the EGM, an analog pulse is generally generated by the EGM logic 7 for input to the credit played hard meter 6 (in some EGMs digital pulses are generated). The jackpot interface board 10 monitors these pulses and sends signals to the jackpot controller 15 via the venue jackpot network 14 to increment the software counter that contains the accumulated number of pulses (absolute value). Once this event occurred, the
10 jackpot interface board 10 sends a communication packet to the jackpot controller 15 that will contain the current time stamp and the software counter. If the venue jackpot network 14 is busy, the jackpot interface board 10 will retry next time. This means that the counter can be incremented more than once between each transmission.

15 In the jackpot controller 15 there is a queue of all counters (contributions) that are received from all participating EGMs 12. The jackpot controller 15 monitors the received counter values from the queue and performs the following steps:

- retrieves the individual EGM counter from jackpot controller's battery backed RAM and calculates the difference between the old value and the new value.
20 Then it replaces the old with the new.
- the calculated difference is added to the jackpot pool that is also stored in its BBRAM.
- the pool is compared to the hidden prize. If the pool is less than the prize, the process continues to the next entry in the queue. If the pool is equal or exceeds
25 the hidden prize, the win process is initiated by the jackpot controller.

In case of a win, the contributions queue is processed until the win process verifies the winning EGM and its software, and the contributions are added to the separate pool. Once the winning EGM is verified, the jackpot is stopped by broadcasting a command with a message
30 ID.

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Every defined period of time the jackpot controller broadcasts the current value of the jackpot pool to all the jackpot interface boards 10 (this comes as a message with message ID). As the amount is in cents, the jackpot controller 15 converts it to a dollar amount and then broadcasts. The jackpot interface boards 10, if configured to do so, will display the value on the EGM displays 2. Similar information may be displayed on the video monitors 23 and LED displays 27.

Referring now to Figures 6 to 12, there is shown therein an exemplary form of interface board 10 constructed in accordance with the invention. The exemplary form of interface board 10 is suitable for coupling to EGMs made by VLC. The operation of the circuit shown will be apparent to those skilled in the art and therefore only a brief outline of the important features of the circuit are mentioned below.

Figure 6 shows the network interface 22 which in this case is a standard ethernet chip. The interface 22 is connected to the connector 72 via a pulse transformer 74 (e.g. NPI5826). Interconnections are also made to the network interface 22 via a local bus 76, a system bus 78, a control bus 80 and an EPLD bus 82 as will be explained in more detail below.

As shown in Figure 7, the system bus 78 provides interconnection to the memory 20 in this case in the form of a flash memory device 90 and RAMs 92 and 94. The system bus 78 also provides connection to EPLD logic circuitry 44 (e.g. EPM 7032-3). The local bus 76 provides coupling between the interface 22 and the RAM 94 which stores data required by the interface 22. The logic circuitry 44 may comprise Flash Programmable Gate Array (EPLD) such as an Altera 7032 array which is set up to provide various logical signals. The logic circuitry 44 essentially provides "glue logic" for the various components of the circuit board 10. As is well understood in the art, the glue logic is concerned primarily with providing signals which have the appropriate polarity, timing, etc. for correct functioning of the circuit. The glue logic could be implemented by discrete components provided on the board. It is, however, desirable to implement them in the programmable array so as to provide economy,

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simplicity of design and flexibility to change circuit details if needed. Some examples of the glue logic functions carried out by the logic circuitry 44 illustrated in Figures 11 to 14.

Figure 8 shows the microprocessor 16 and its interconnections with the system bus 78 and a control bus 80. The microprocessor 16 may comprise an NEC V25 processor. The microprocessor produces output signals for the video bus 102 which is coupled to the video mixing device 42 (Figure 10) and to other components which are shown in Figure 9 via an EGM input/output bus 104. The microprocessor 16 also handles the control and formatting of serial data signals (pins 41, 43, 44, 45, 46 and 47) for the communications bus 28. Serial data from the microprocessor 16 is connected to output connectors 108 and 110 via converters 103 which convert TTL level outputs into a balanced drive required for the RS 422 serial link. The circuit also includes converters 105 which convert RS 422 inputs into TTL compatible signals required by the microprocessor 16. Termination resistors 107 and 109 are provided for the connectors 108 and 110 respectively. The circuitry also includes input protection diodes 111 and 113 for the connectors 108 and 110 respectively. Figure 8 also shows an oscillator circuit 115 which produces 60 MHz clock pulses for the board 10.

Figure 9 shows an input/output connector 120 which is used to couple the board 10 to the input signals generated by the EGM logic 7 to drive the hard meters 6 of the EGM. The connector 120 is coupled to the EGM input/output bus 104 via coupling resistors 122. Input protection diodes 121 are provided across the various input lines of the connector 120. In alternative embodiments, the coupling resistors 122 may be replaced by opto-coupling circuits.

The hard meter input signals include: (i) credit played on line 123, (ii) cash out on line 125, (iii) cash in on line 127, and (iv) credit won on line 129, the hard meter output signals on lines 123, 125, 127 and 129. In some types of EGM the hard meter signals are output in serial form, and in those instances a serial to parallel conversion is necessary in order to derive the individual signal lines.

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Figure 9 also shows a connector 131 to which connections are made from the door seal switch 9, audit key 43 and logic seal 41. The circuit includes a relay having a coil 133 for operating the contacts 45. The contacts 45 are connected in series in line 126 which leads to the door seal switch 9, as also shown in Figure 4. The contacts 45 are normally closed.
5 When, however, the microprocessor 16 has been informed of a jackpot by the jackpot controller 15, it produces an appropriate signal on the bus 104 to deactivate the coil 133 and open the contacts 45. The EGM logic 7 responds to this and stops normal play as required.

Figure 9 also shows an input line 137 which is coupled to the logic seal switch 41
10 through the connector 131. The line 137 is coupled to an 8-bit latch 139 (e.g. 74HCT299) which provides additional security so that the effect of the logic seal switch 41 cannot simply be shorted out. The microprocessor 16 writes an 8-bit number into data lines (d_0 - d_7) from system bus 78 and this is stored in the latch. If the state of the switch 41 changes the latch 139 will be reset and this will be sensed by the microprocessor, thus indicating that the logic seal
15 has been broken. Opening of the switch 41 will also be sensed by the EGM logic 7. The circuit also includes a memory supervisor chip 141 which operates to provide power to the memory 90 from the normal power supply or from backup batteries. The circuit 141 also provides power for the latch 139 and this provides additional security by preventing tampering with the latch 139 when power is off.

20

The circuit also includes a memory supervisor chip 143 which controls normal power or backup power to the memory 92 (see Figure 6). A further memory supervisor chip 145 is provided to control the backup battery for the memory 94. The chip 145 also monitors the power supply to the microprocessor 16 and enables the microprocessor 16 to backup various
25 parameters before power is lost. The chip 145 also includes a watchdog circuit. The program in memory 20 is required to cause the microprocessor 16 to reset the watchdog of chip 145 within a certain period of time. If this is not done, then the chip 145 causes a reset of the microprocessor 16. This provides a recovery mechanism should the microprocessor become "lost" for any reason. The chip 145 may comprise an MAX690 and the chips 141 and 143 may
30 comprise a DS1210S.

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The video mixing device 42 is shown in greater detail in Figure 10. The device 42 includes a video character generator 138 and a video multiplexer 150. The character generator 138 is connected via the video bus 102 to a video input connector 140 which receives the current video output of the EGM 12 to which the board 10 is connected. In the illustrated
5 circuit, the multiplexer 150 comprises a digital multiplexer which is appropriate for a digital video display. This circuit operates to overlay or substitute video character signals produced by the generator 138 on or for the normal EGM video display received at the video input connector 140 and provide these signals to the video output connector 144 to which the EGM display 2 is connected. The video character generator 138 may comprise an NEC UPD 6453
10 circuit and the multiplexer 150 may comprise a 74HC157 circuit.

Figure 11 diagrammatically illustrates the glue logic implemented by the logic circuit 44. Briefly, the logic includes an intelligent dividing device 160 which receives horizontal and vertical sync pulses from the EGM video via the video input connector 140 on lines 162 and
15 164. The device 160 is arranged to always produce negative going outputs, which is appropriate for the rest of the circuitry. If the inputs are already negative then the sync pulses are simply passed to the output. If the input sync pulses are positive, the pulses are inverted at the outputs. The selection is made by a stored input from the microprocessor 16 which is set for particular machinery.

20

The circuitry of Figure 11 includes a divider circuit 166 which receives 60 megahertz clock pulses from the oscillator 115 and produces a 20 MHz output on line 168 and anti-phase
15 MHz outputs on the lines 170 and 172. The clock pulses on line 168 are inputted to the network interface circuit 22 and the clock pulses on the lines 170 and 172 are inputted to the
25 microprocessor 16. Figure 13 shows the divider circuit 166 in more detail.

The circuit also includes a memory decode device 174 which has inputs on lines 176 from the microprocessor. The memory decode device produces outputs on lines 178 which provide control signals for the memories 90 and 92, for the logic seal components 139 and 141
30 and for an expansion port 180, as seen in Figure 7. Figure 14 illustrates in more detail the

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memory decode device 174.

The circuit of Figure 11 includes an array of gates 182 having input lines 184 from the microprocessor 16. The gates 182 serve to provide output signals on lines 186 which are
5 coupled to the network interface 22 to provide signals in the appropriate format for writing to and from the network interface 22 and to the memory 92.

The circuit of Figure 11 also includes an inverter 188 which receives a power fail signal on line 190 and operates to provide an inverted output.

10

The circuit of Figure 11 also includes a NOR gate 192 which receives input on line 194 from the character generator 138 and on line 196 from the microprocessor 16. The output line 198 of the gate 192 is inputted to the multiplexer 150. The arrangement is such that the signal on line 196 from the microprocessor operates to determine whether the normal signal display
15 from the EGM in the video input will be blanked out when the character information from the character generator 138 is displayed. Alternatively, the information generated by the character generator 138 can be superimposed on the normal EGM video display.

It will be appreciated by those skilled in the art that the arrangement of Figures 7 and
20 10 provides a convenient and flexible arrangement for superimposing video character information on the video output displays of various types of EGMs. In other words, with essentially the same basic circuit configuration for the interface board 10, it can provide video superposition with different types of EGMs.

25 Figure 15 diagrammatically illustrates the manner in which the board 10 is connected to the EGM logic 7.

Figure 16 is a flow chart showing typical steps in the boot loading of the memory 20 of the board 10 on receipt of appropriate signals from the jackpot controller 15. The flow
30 chart includes a question box 200 to determine if an initialising message JIB_INIT is received

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from the jackpot controller 15. If yes, the program executes an initialisation sequence indicated by step 202. The flow chart includes a question box 204 which determines if a message is received (JIB_DOWNLOAD) signal is received from the jackpot controller 15 to download jackpot configuration data from the jackpot controller 15 into the memory 20 of the board 10, as indicated by the step 206. This step in the program can be used to update or load new software into the board 10 under the control of the jackpot controller 15. The flow chart includes a question box 208 which determines if a reset message JIB_RESET message is received from the jackpot controller 15. If yes the board 10 is reset as indicated by step 210. It will be appreciated from the above that once the program of step 206 has been implemented, the board 10 is ready to participate in a jackpot together with other EGMs which have been programmed in a similar way subject to the control of the jackpot controller 15.

The boot loading program may also include provision of a procedure for initiating encryption of communications between the JIB and the jackpot controller in response to an "encrypt" message and encryption key from the jackpot controller, although those steps are not illustrated in the flowchart of Figure 16.

Figure 17 is a flow chart showing steps in the main programming loop 212 which is executed by the microprocessor 16. The main loop 212 is executed after boot loading of the board 10, as described above. The main loop includes a question box 214 which enquires whether any commands have been received from the jackpot controller 15. If yes, the command is performed as indicated by step 216 and an acknowledgment is given to the jackpot controller 15 as indicated by step 218. If no, an enquiry is made by question box 220 to see if the jackpot controller has communicated with the board 10 recently. If no, then a logical decision is made that a communication has been lost, as indicated by step 222 and steps are taken to stop checking the hard meter outputs of the EGM logic 7. If the response to question box 220 is yes, the program passes to step 224 which updates timed messages for the EGM 10. The program then passes to question box 226 which monitors the hard meter inputs and also senses changes to other inputs such as logic seals and the like. If a change has occurred, the appropriate steps will be taken as indicated in step 228. If the step is an

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increment in the hard meter, the step 228 will cause appropriate signals to be sent to the jackpot controller 16. If other inputs have changed such as a logic seal being broken, then this causes stopping of the operation of the EGM and appropriate signalling to the jackpot controller 15. If the response to the question box 226 is no, the program passes to question box 230 which enquires whether the board 10 has transmitted signals to the jackpot controller 15 recently. If no, the program passes to step 232 which causes a message to be sent to the jackpot controller 15 indicating that the board 10 is still operating. If the response to question box 230 is yes, the program returns to the first question box 214.

10 The flow chart of Figure 18 illustrates in more detail an EGM monitoring loop 234 which is carried out in the step 228. The loop 234 includes a question box 236 which enquires whether the hard meter input pulse is bad, that is to say to see if the pulse shape does not fit certain preconfigured parameters. If yes, the program passes to step 238 which activates a bad pulse event which is transmitted to the jackpot controller 15 so that appropriate action can be
15 taken. If the response to question box 236 is no, the program passes to question box 240 which enquires whether the hard meter has become disconnected. This effectively checks to see if the hardware circuitry recognises a disconnection. If yes, the program passes to step 242 which activates a meter disconnected event and this is signalled to the jackpot controller 15 which causes discontinuance of participation of the EGM in the jackpot. If the response
20 to question box 240 is no, the program passes to question box 224 which enquires whether a predetermined number of consecutive hard meter pulses has occurred. If the response is yes, the program passes to step 246 which activates the hard meter's consecutive event which may be flashing selected displays on the EGM screen while hard meters are being ticked (i.e. being incremented). If the response to question box 244 is no, the program passes to question box
25 248 which enquires whether the number of consecutive pulses has exceeded a predetermined runaway limit. If yes, the program passes to step 250 which activates a runaway event sequence for the meter and this again will be signalled to the jackpot controller 15. If the response to question box 248 is no, the program passes to question box 252 which enquires whether the number of pulses has reached the configured threshold. If yes, the program passes
30 to step 254 to activate the meter's delta event. The delta event may be activated when a

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predetermined number of hard meter pulses have been counted. Typically this may be, say, three meter counts. In this case, the board 10 would not send a message to the jackpot controller 15 until either three meter counts had been received or it was time to send a message (i.e. to communicate with the jackpot controller 15 to let it know that the EGM is still
5 active. This prevents rapidly sending many messages to the jackpot controller 15, each indicating one meter pulse when the meters are being incremented quickly. If no, the program will pass to question box 230.

Whilst the board 10 is active the main program loop 212 will continue to operate and
10 carry out the functions described above.

The described arrangements have been advanced merely by way of explanation, and many modifications and variations may be made thereto without departing from the spirit and scope of the invention.

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CLAIMS:

1. A jackpot interface for connection to an electronic gaming machine (EGM) which includes a video display, a hard meter, and EGM logic for generating first video signals for
5 said video display and hard meter input signals for said hard meter, said EGM being adapted to play an independent game and participate in a multiple EGM jackpot game, wherein the jackpot interface comprises:
- a hard meter monitor which monitors said hard meter input signals for communication to a controller for determination of a jackpot award;
- 10 video generating means for generating second video signals relating to said jackpot award; and
- combining means for causing the second video signals to be superimposed on or replace the first video signals to thereby display on said video display messages relating to said jackpot award.
- 15
2. A jackpot interface as claimed in claim 1, wherein the jackpot interface comprises a circuit board which is adapted for connection to an otherwise standard electronic gaming machine.
- 20 3. A jackpot interface as claimed in claim 1 or 2, wherein the combining means comprises a video multiplexing device which receives said first and second video signals and has an output coupled to said video display.
4. A jackpot interface as claimed in claim 1, 2 or 3, wherein the EGM includes at least
25 one EGM disable circuit for generating disable signals, the EGM logic being responsive to said disable signals to stop playing of independent games, and wherein the jackpot interface includes logic circuitry for generating, in response to a jackpot award, a signal which is transmitted to the EGM logic and which is interpreted by the EGM logic as a disable signal, thereby stopping independent game play on the EGM.

30

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5. A jackpot interface as claimed in claim 1, further comprising networking circuitry for communicating first data messages containing information relating to said hard meter input signals to the controller and receiving second data messages containing information relating to said jackpot award.

5

6. A jackpot interface as claimed in claim 5, wherein the jackpot interface is responsive to said second data messages to generate said second video signals for display on said video display.

10 7. A jackpot interface as claimed in claim 6, wherein said second video signals are effective to display a message, when displayed on said video display by said combining means, which represents information contained in said second data messages.

8. A jackpot interface as claimed in claim 7, wherein the message displayed by said
15 second video signals is a multiple EGM jackpot amount.

9. A jackpot interface as claimed in claim 8, wherein the message displayed by said second video signals indicates the jackpot amount being awarded to a player at said EGM.

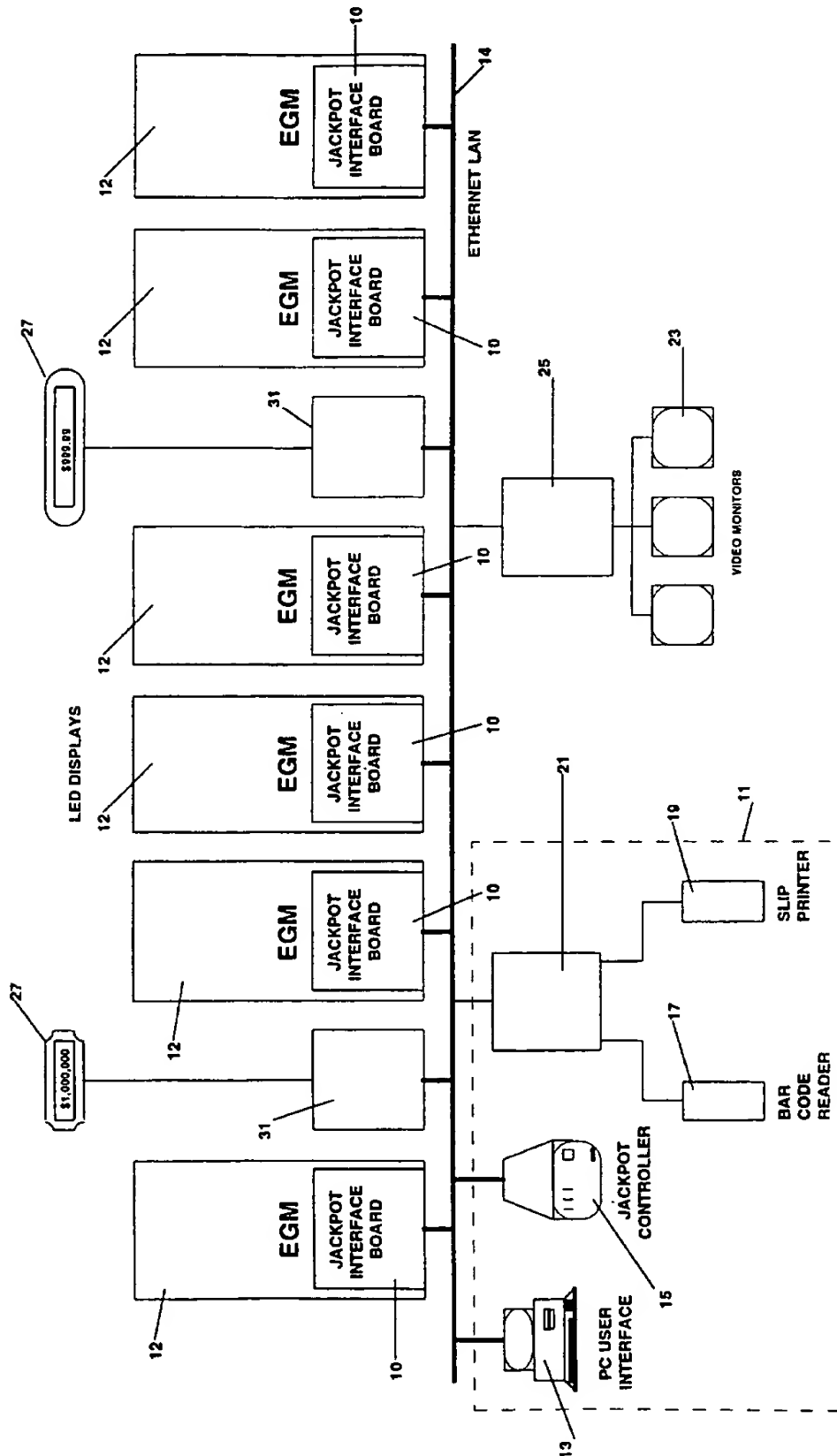
20 10. A jackpot interface board for use in an electronic, gaming machine (EGM) having a video display, hard meters and EGM logic for generating first video signals for said video display and hard meter input signals to said hard meters, said jackpot interface board including monitoring means for monitoring hard meter input signals generated by the EGM logic and transferring said hard meter input signals for addition to a jackpot pool for determining when
25 a jackpot pool is won, video generating means for generating jackpot video signals and video combining means for causing said jackpot video signals to be superimposed upon the video display when a jackpot has been won.

11. A jackpot interface board as claimed in claim 10, which is adapted for connection to
30 an otherwise standard EGM.

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12. A jackpot interface board as claimed in claim 10 or 11, wherein said EGM is adapted for playing of an independent game and participation in said jackpot pool through the jackpot interface board, said jackpot interface board being arranged for communication with an external controller for sending and receiving data relating to said jackpot pool, and wherein
5 the jackpot interface board is coupled to the EGM to suspend playing of said independent game in response to receipt of data indicating an award of said jackpot pool.

13. A jackpot interface board as claimed in claim 12, wherein the suspension of said independent game on the EGM is achieved by simulation by said jackpot interface board of
10 a disable signal of the EGM.



VENUE CONFIGURATION
FIG 1

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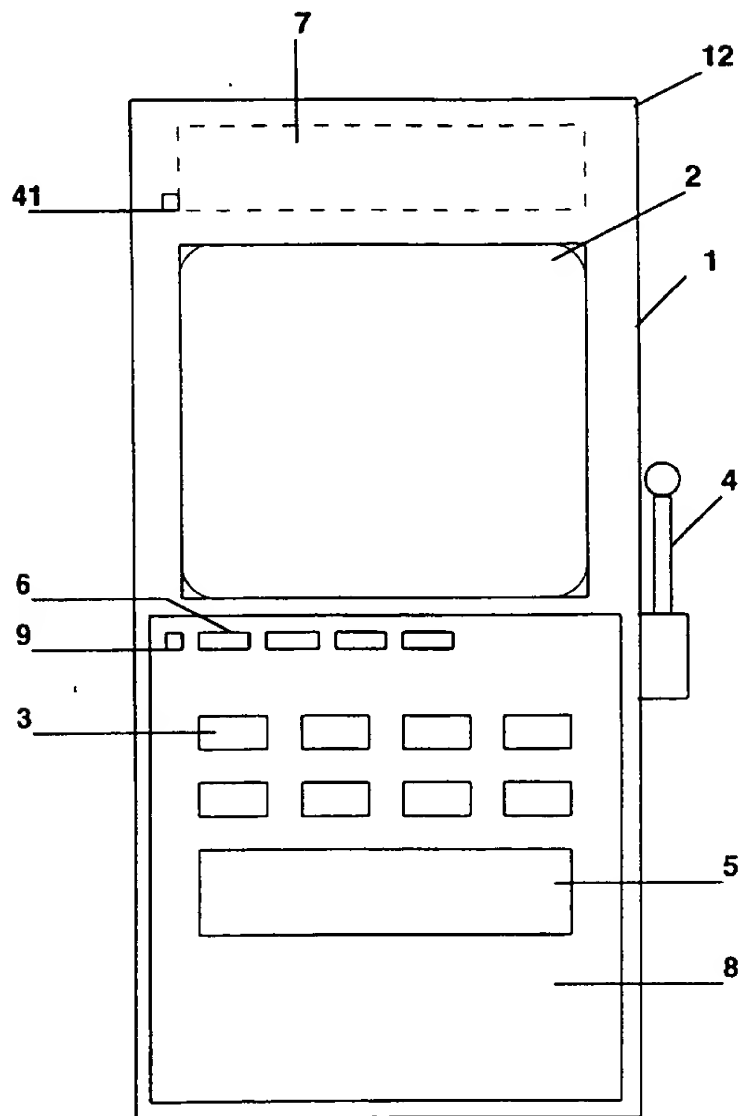


FIG 2

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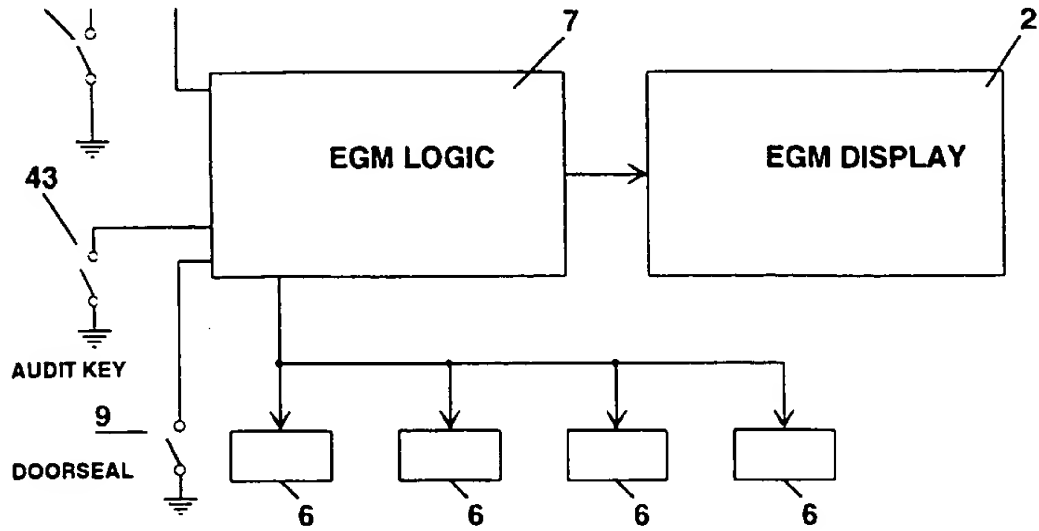


FIG3

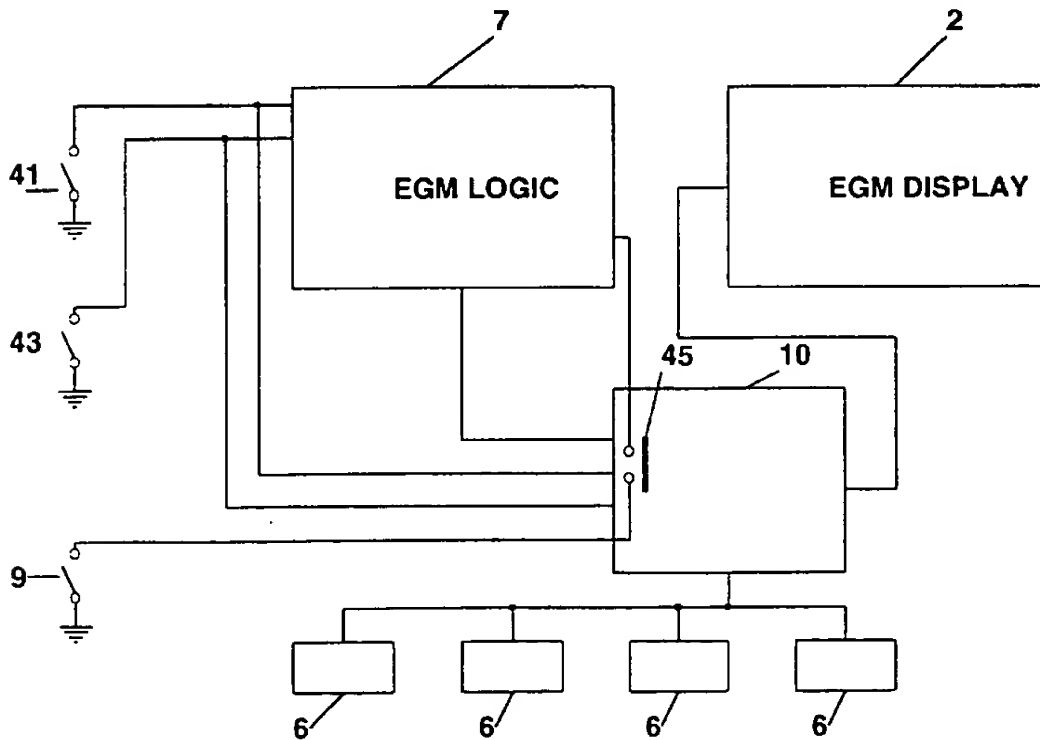


FIG4

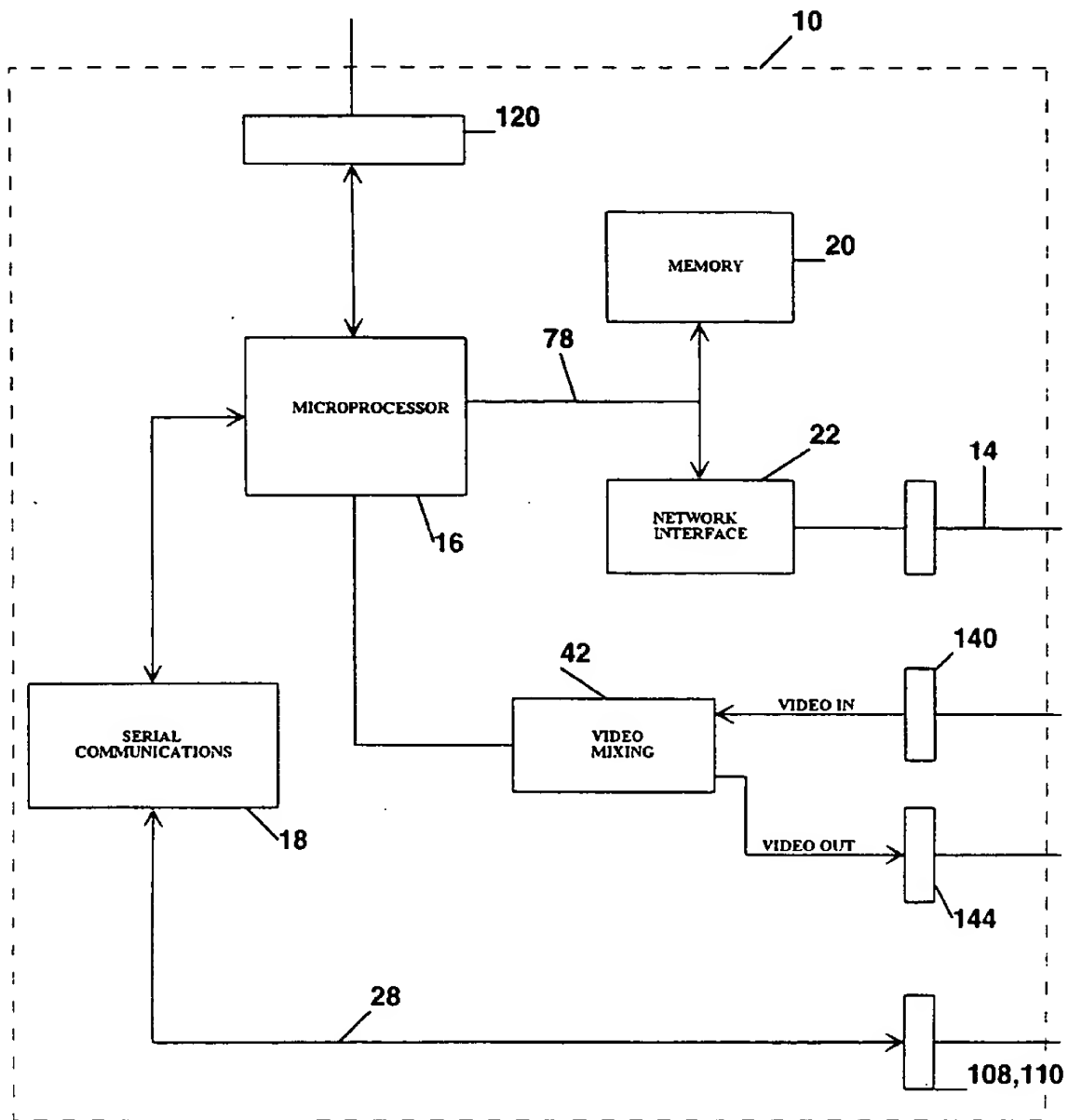


FIG 5

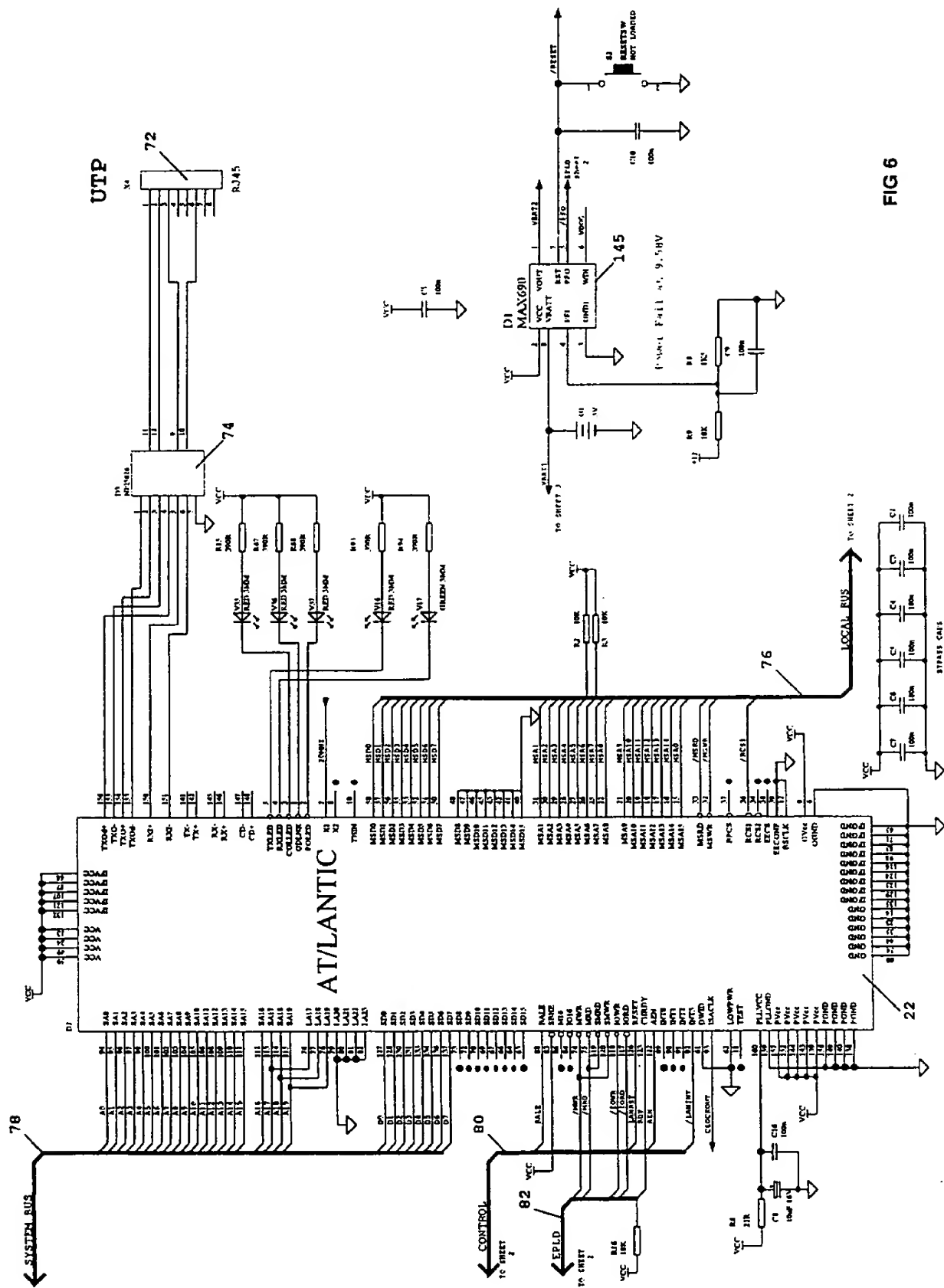


FIG 6

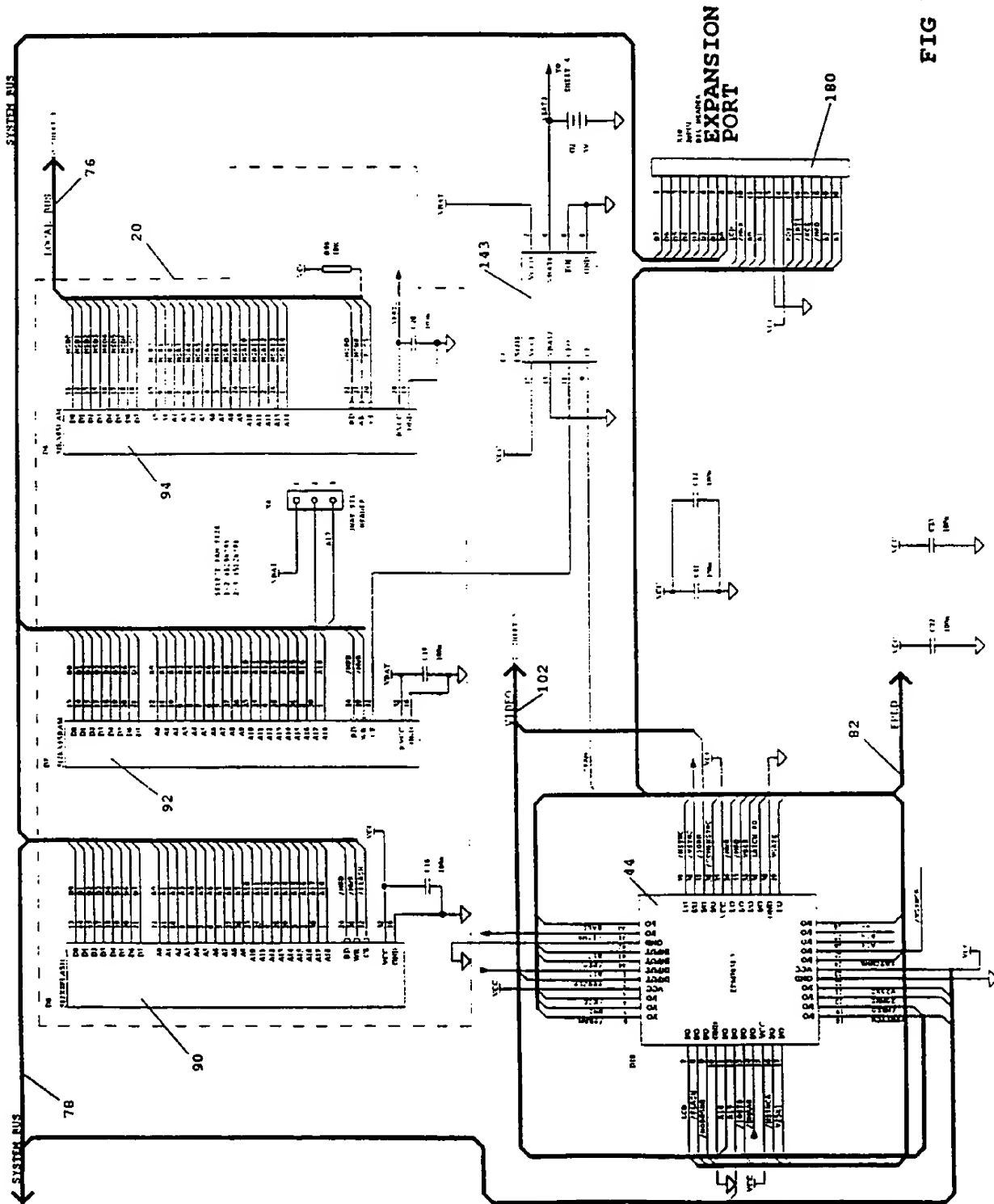


FIG 7

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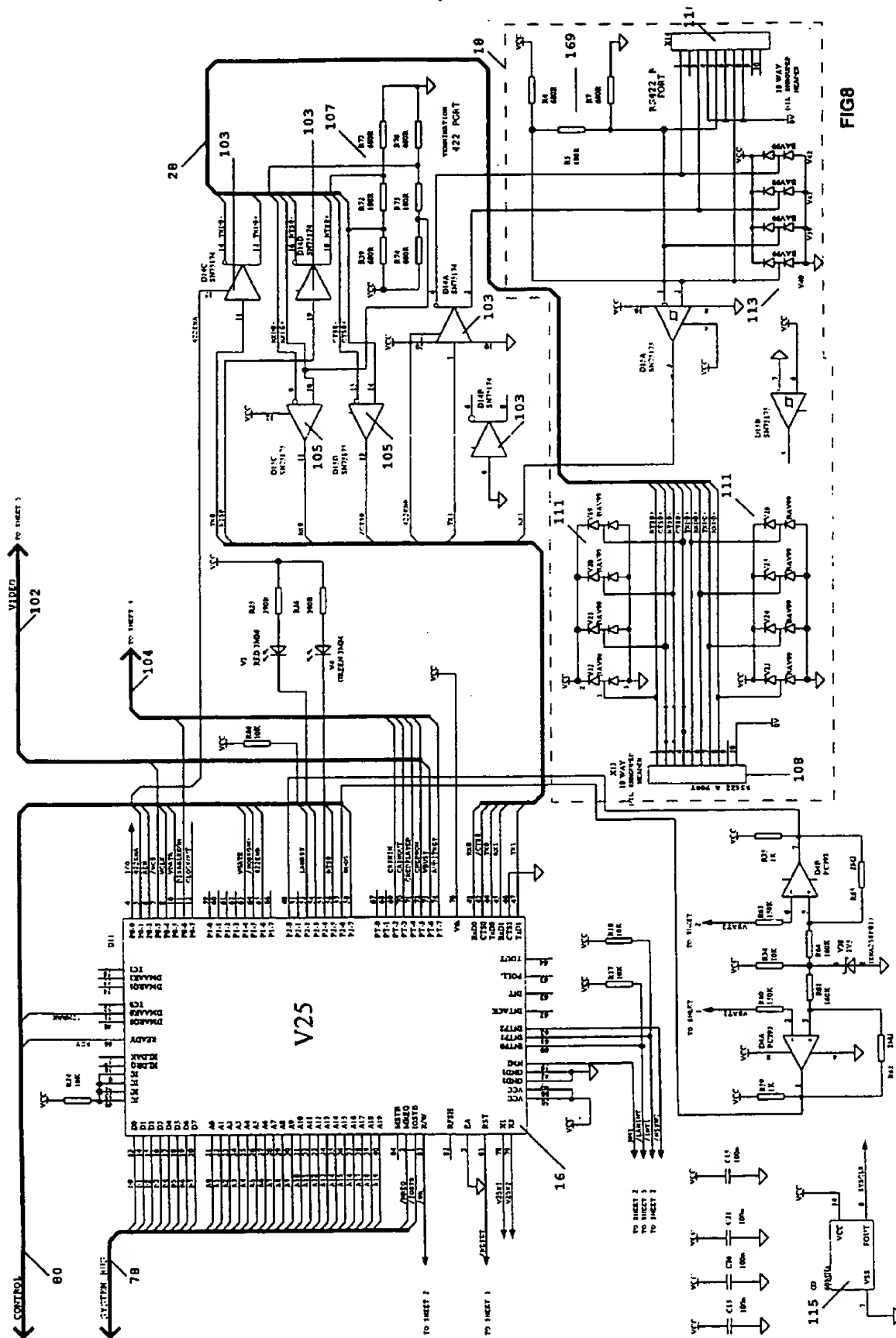


FIG 8

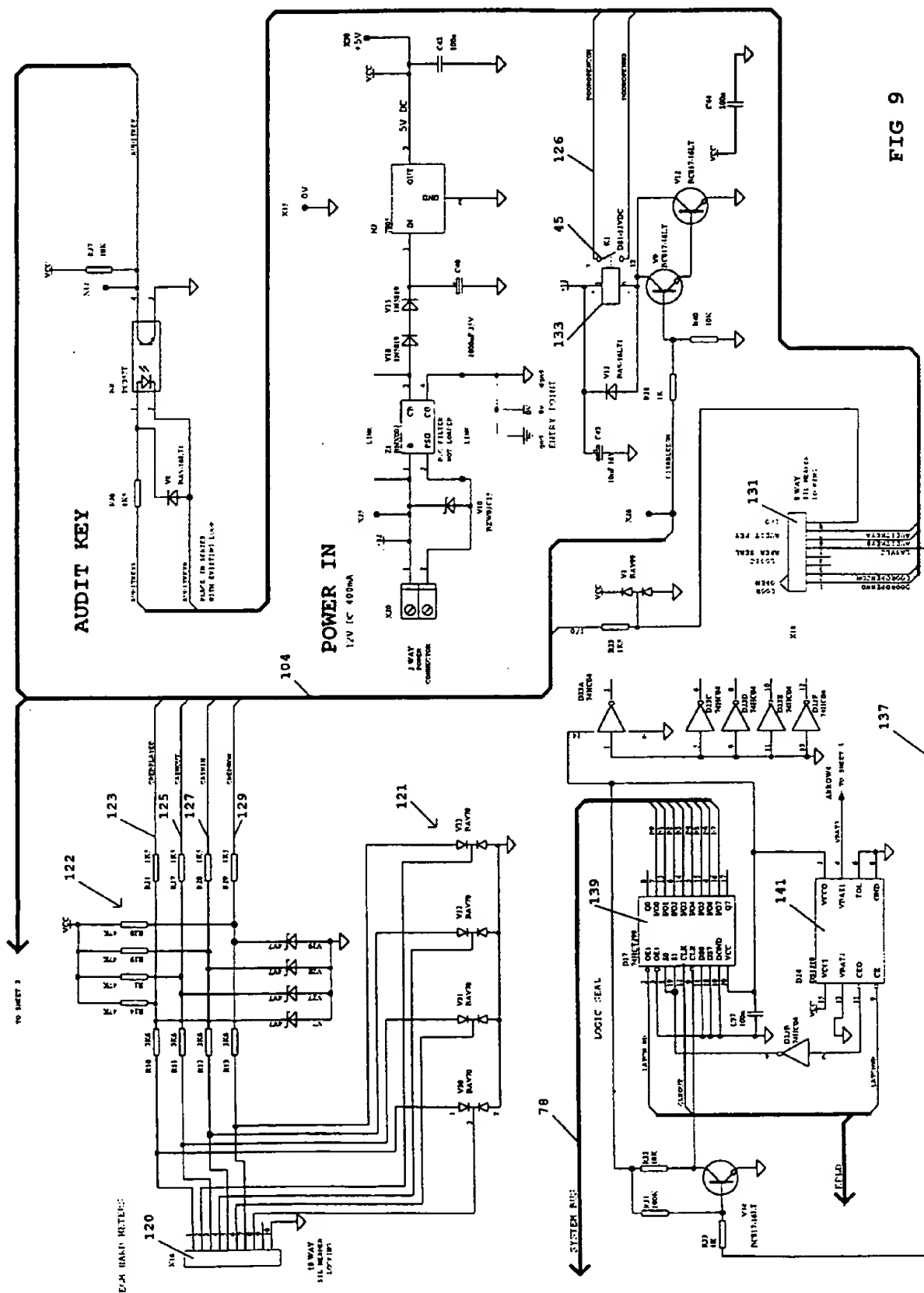


FIG 9

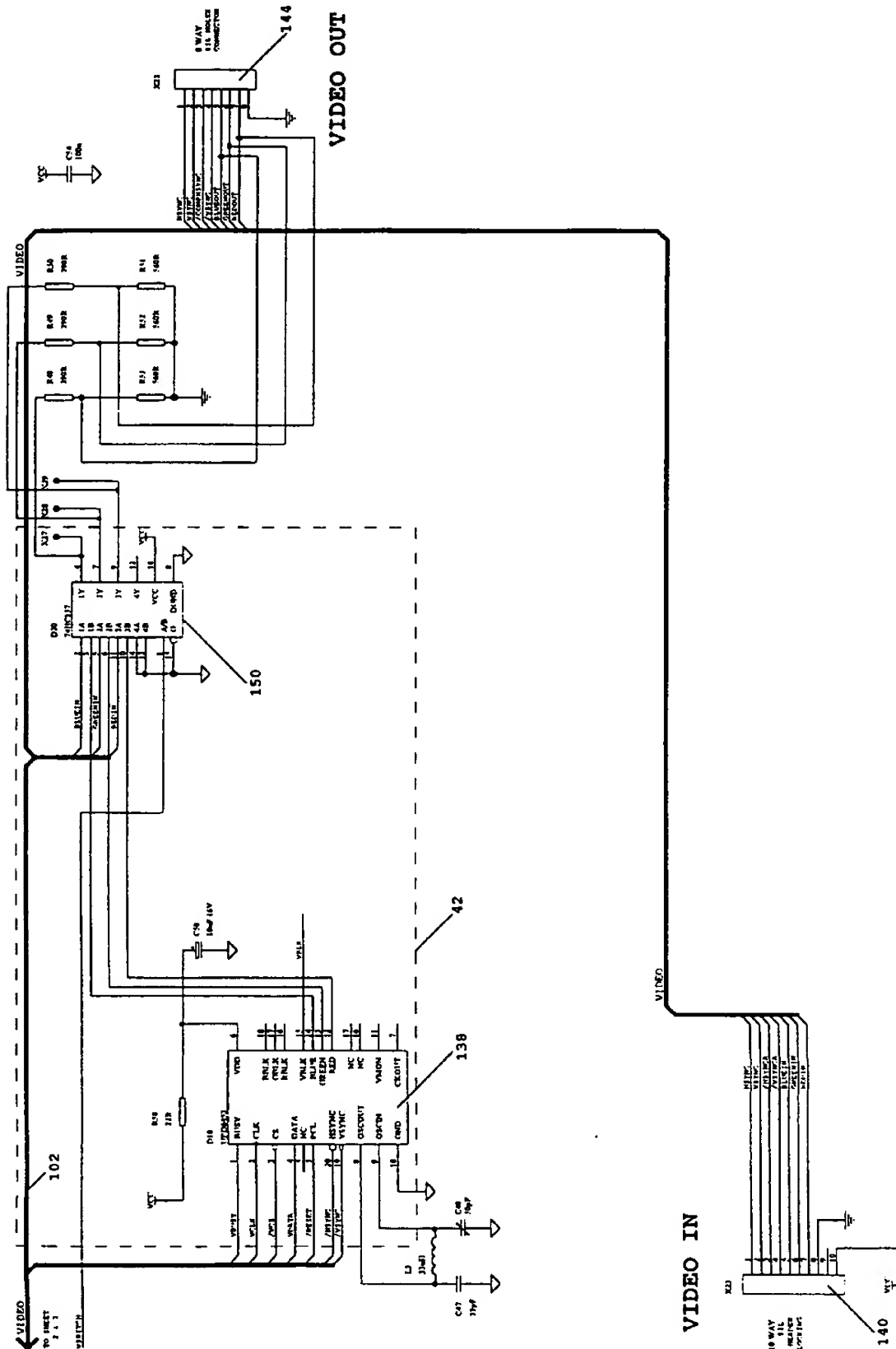


FIG 10

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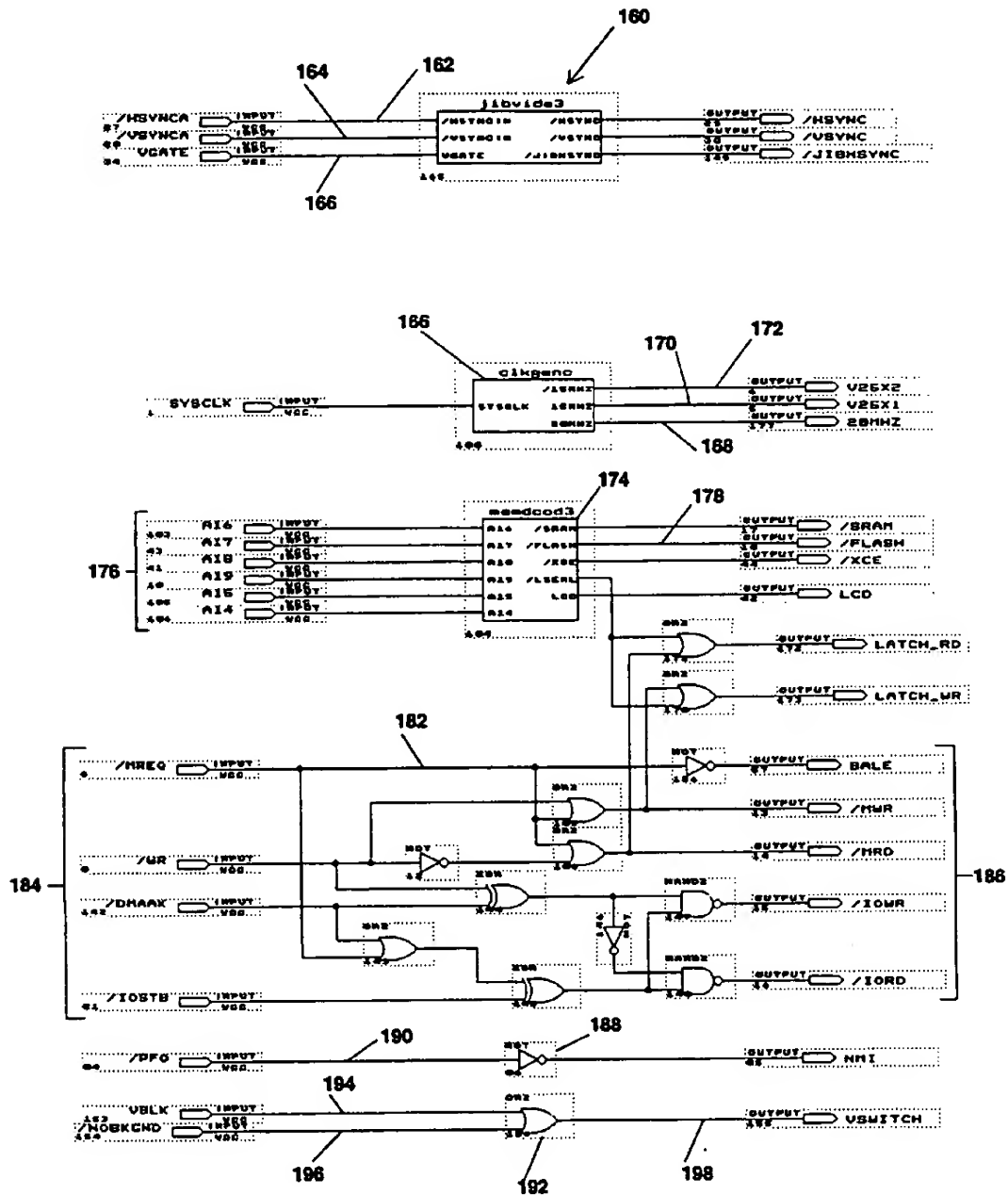


FIG 11

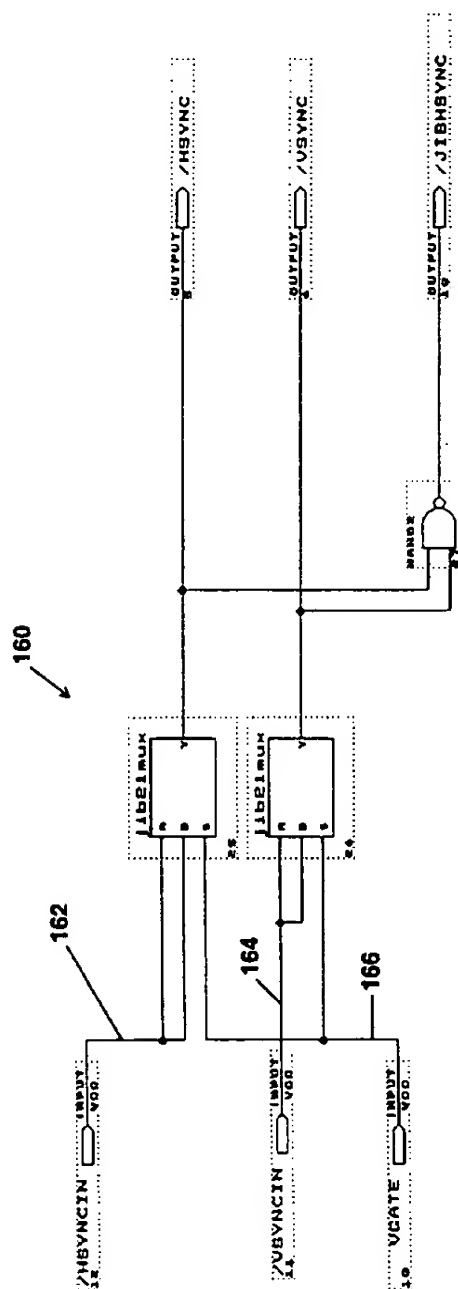


FIG 12

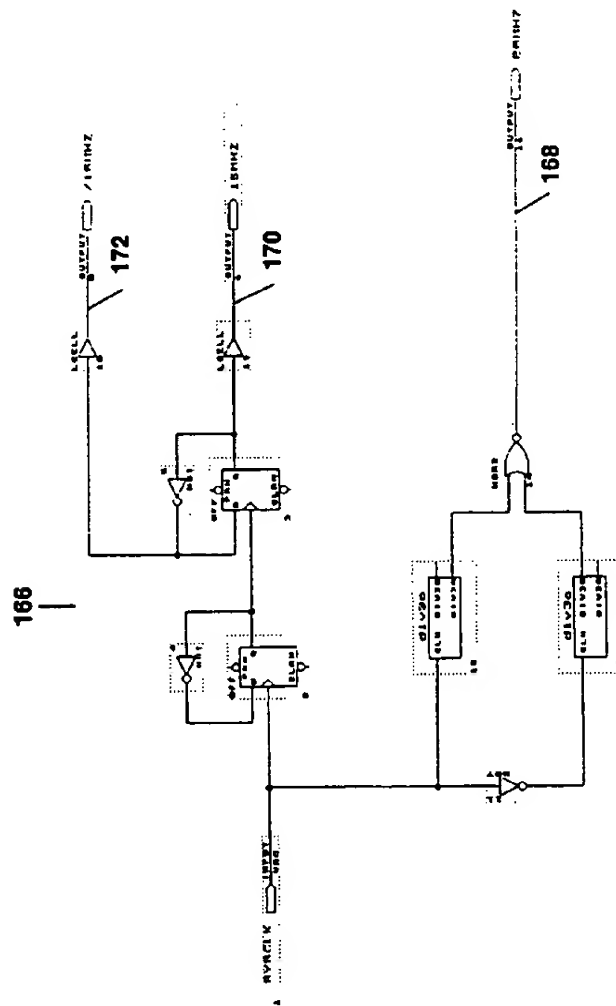
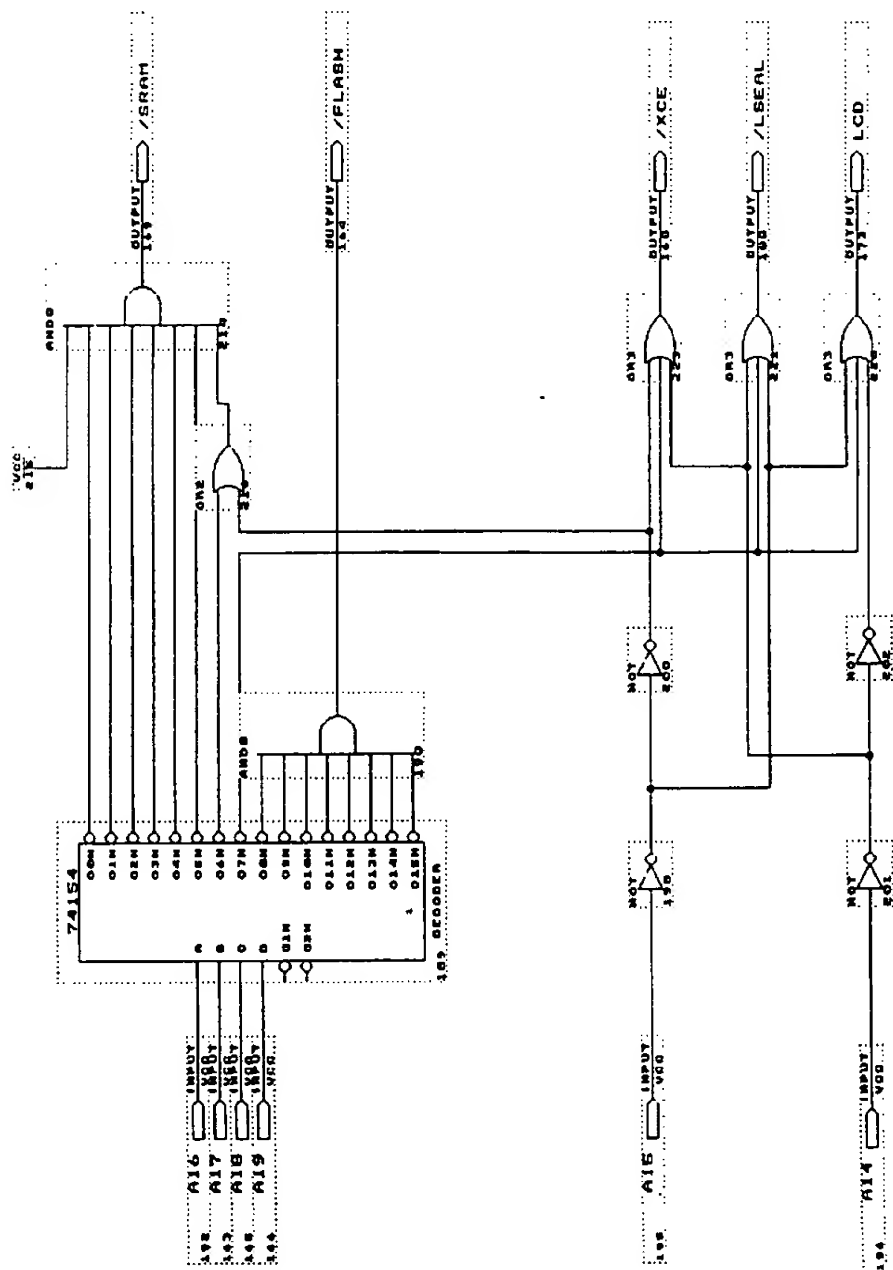
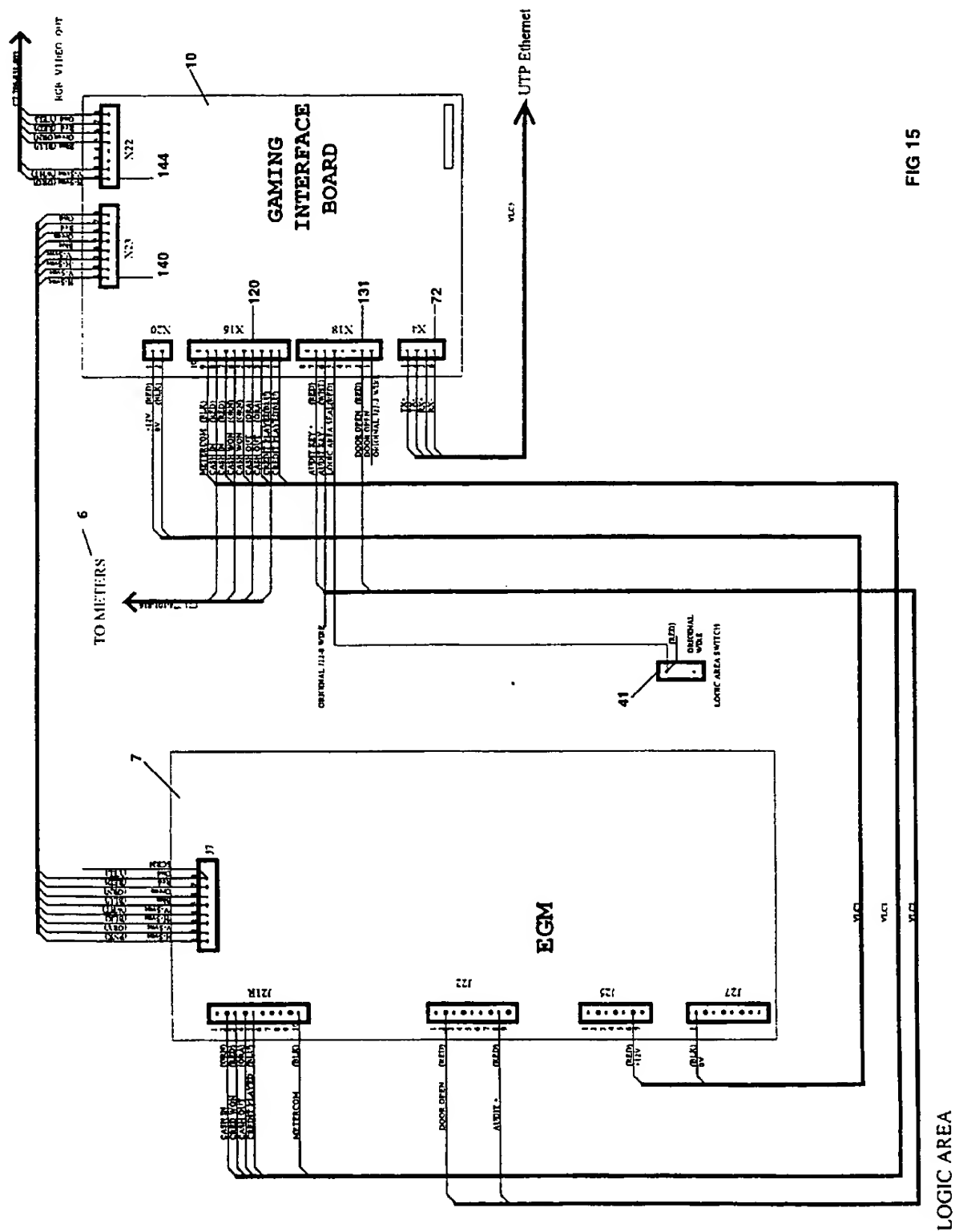
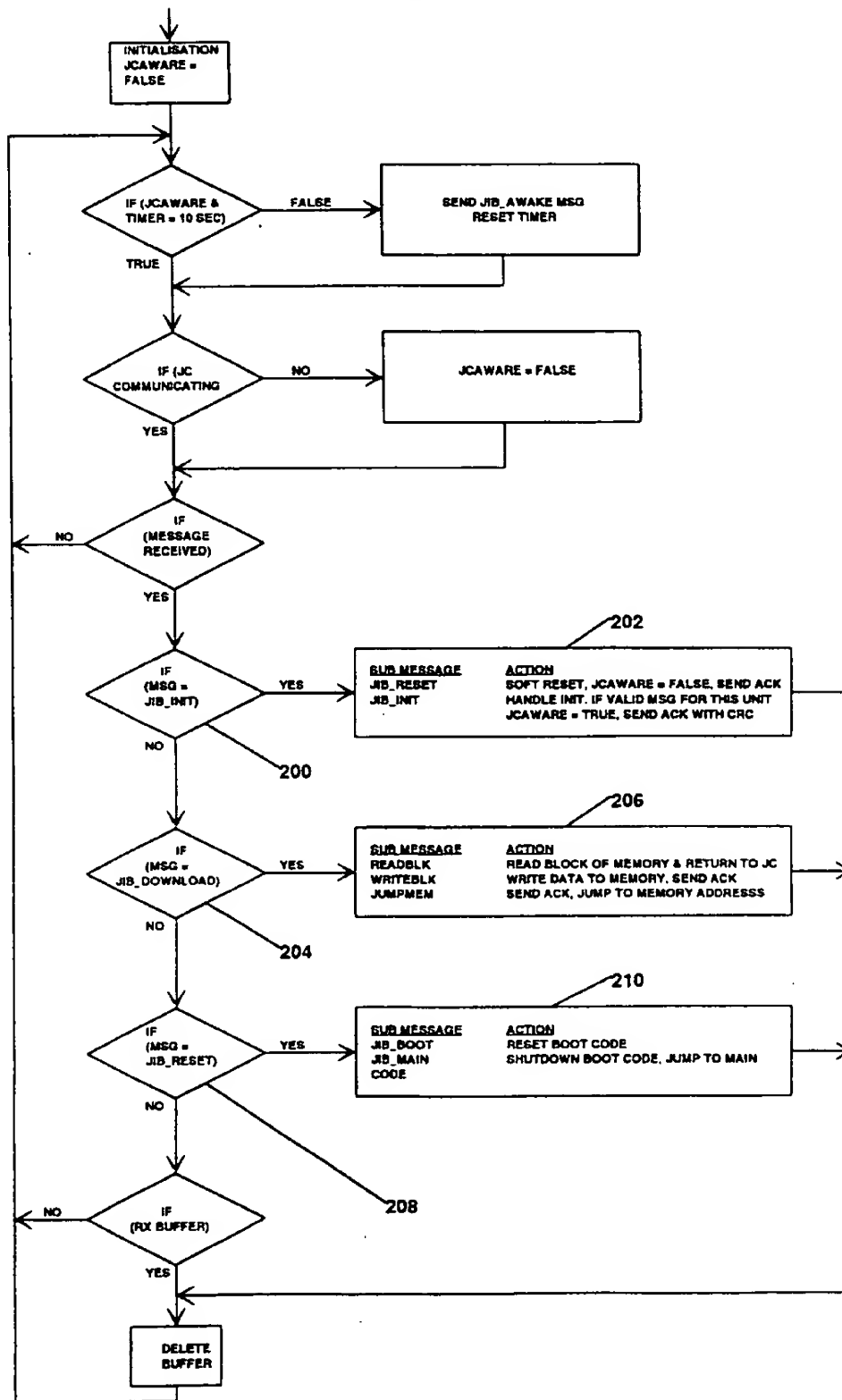


FIG 13



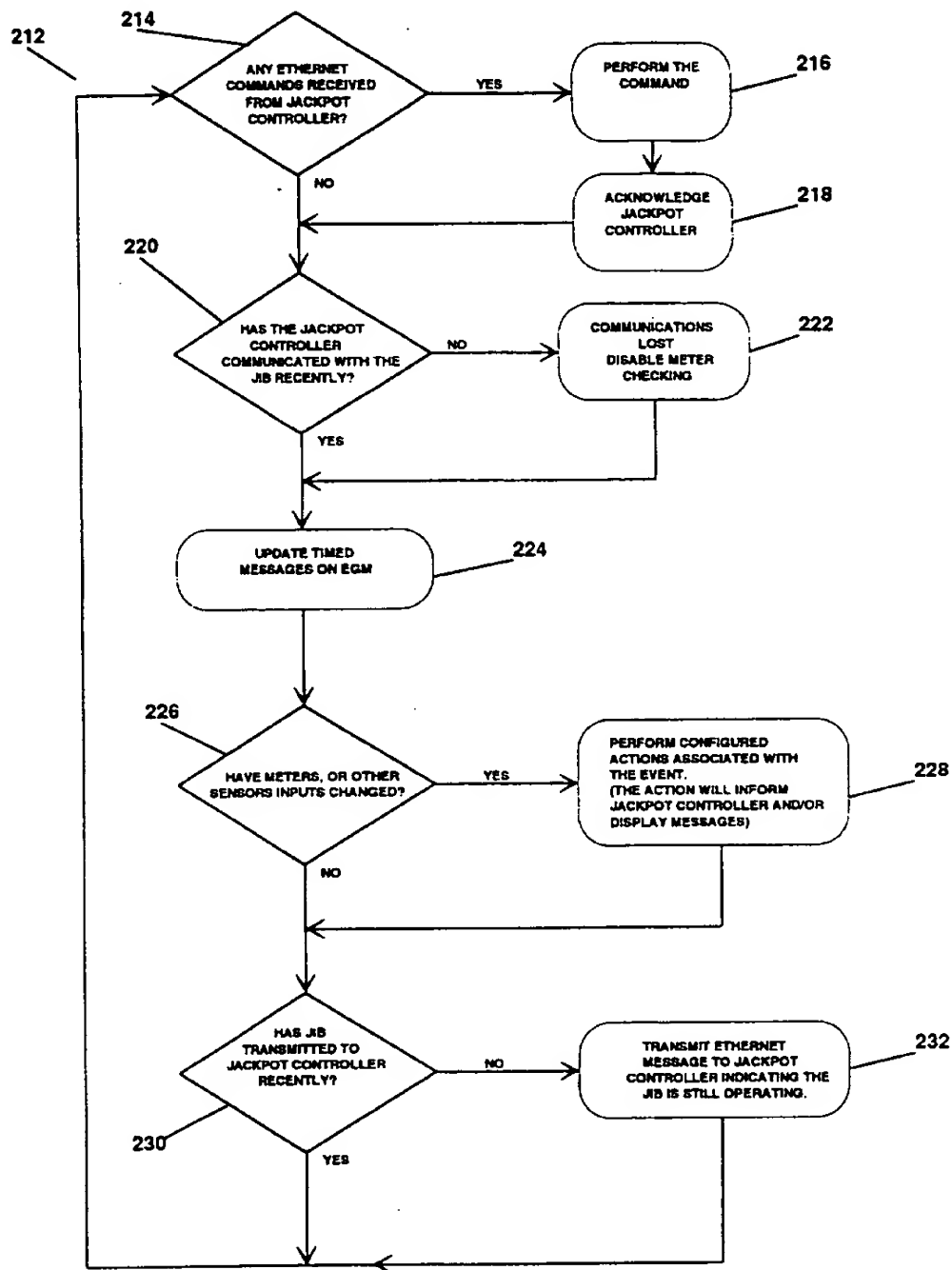


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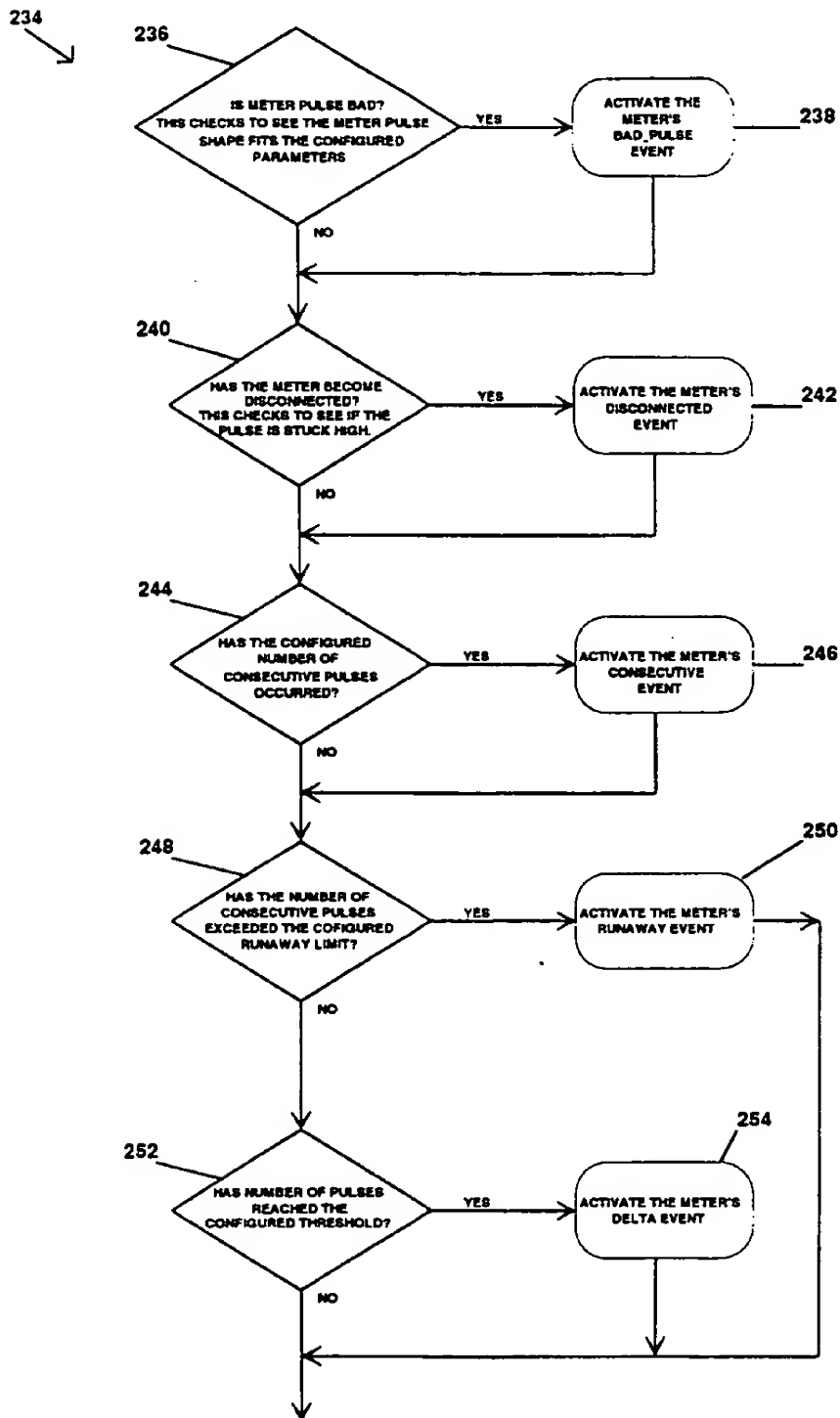
JACKPOT INTERFACE BOARD-BOOT LOADER

FIG 16



JIB MAIN LOOP

FIG 17



EGM METER MONITORING

FIG 18

SUBSTITUTE SHEET (RULE 26)

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/AU 96/00609

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl^b: G06F 3/14, H07N 5/262, A63F 9/22, G06F 19/00 G06F 161:00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G07F 17/32 G07F 17/34 G06F 15/44 G06F 19/00 G06F 161:00 A63F 9/00 A63F 9/22 H04N 5/262, H04N 5/265 H04N 5/272 H04N 5/275 G06F 3/14, G06F 3/147 G06F 3/153

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

AU: IPC AS ABOVE [US: 273/-]

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPAT, CLMS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5398932 A. (EBERHAROT et al) 21 March 1995 Column 4 lines 26/44	1-13
A	US 5353068 A (MORIWAKE) 4 October 1994 Whole document	1-13

☒ Further documents are listed in the continuation of Box C

☒ See patent family annex

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search

29 November 1996

Date of mailing of the international search report

29 -11- 96

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C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5324035 A (MORRIS et al) 28 June 1994 Column 1 lines 56/62, column 2 lines 51/60 Column 5 lines 36/45, column 14 lines 35/50	1-13
A	US 5280909 A (TRACY) 25 January 1994 Column 1 lines 9/14, 46/58 Column 4 lines 29/43 Column 5 lines 34/35, column 9 lines 47/51	1-13
A	US 5116055 A (TRACY) 26 May 1992 Column 1 lines 8/40	1-13
A	US 5048833 A (LAMLE) 17 September 1991 Column 2 lines 13/28	1-13
A	US 4947257 A (FERNANDEZ et al) 7 August 1990 Whole document	1-13
A	US 4872056 A (HICKS et al) 3 October 1989 Whole document	1-3
A	US 4780709 A (RANDALL) 25 October 1988 Whole document	1-13
A	US 4602286 (KELLAR et al) 22 July 1986 Whole document	1-13

INTERNATIONAL SEARCH REPORT

International Application No.

Information on patent family members

PCT/AU 96/00609

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report				Patent Family Member			
US	5398932	AU	13379/95	WO	9517233	US	5505449
US	5353068	EP	586140	JP	6086162		
US	5324035	AU	57333/94	CA	2128715	EP	627949
		WO	9412256				
US	5280909						
US	5116055						
US	5048833	EP	444932	MC	2229		
US	4947257	US	5068650				
US	4872056						
US	4780709	CN	87100869	FR	2595241	GB	2186470
		JP	62191918				
US	4602286	DE	3300959	FR	2520176	GB	2113950
		GB	2157121	GB	2157122	HK	296/91
		HK	297/91				
END OF ANNEX							